WHAT IS CLAIMED IS:

1. An MPEG on-screen display coder comprising:

an on-screen display turn on device arranged to provide an output when an on-screen display is to be turned on; and,

an MPEG encoder arranged to encode frames with the on-screen display in response to the output of the on-screen display turn on device.

2. The MPEG on-screen display coder of claim 1 wherein the MPEG encoder replaces original video frames with the encoded frames, and wherein the frames encoded with the on-screen display have a time base which is independent of the original video frames.

3. The MPEG on-screen display coder of claim 2 wherein the on-screen display is overlaid on a solid color background.

4. The MPEG on-screen display coder of claim 2 wherein the MPEG encoder is arranged to calculate a video hold off time dependent upon a number of frames in a decoder buffer of a digital television and to use the video hold off time so as to prevent overflow of the decoder buffer.

5. The MPEG on-screen display coder of claim 4 wherein the MPEG encoder supplies the video hold off time to the on-screen display turn on device, and wherein the on-screen display turn on device permits the frames encoded with the on-screen display to be supplied to the digital television when the video hold off time expires.

6. The MPEG on-screen display coder of claim 1 wherein the MPEG encoder replaces original video frames with the encoded frames, and wherein the frames encoded with the on-screen display have a time base which is slaved to the original video frames.

7. The MPEG on-screen display coder of claim 6 wherein the on-screen display is overlaid on a solid color background.

8. The MPEG on-screen display coder of claim 6 wherein the MPEG encoder is arranged to supply first and second I frame markers to the on-screen display turn on device, wherein the on-screen display turn on device causes the frames encoded with the on-screen display to be supplied to a digital television in response to the first I frame marker, and wherein the on-screen display turn on device causes the original video frames to be supplied to the digital television in response to the second I frame marker.

9. The MPEG on-screen display coder of claim 6 wherein the MPEG encoder is arranged to supply a video I frame marker and an on-screen display I frame marker to the on-screen display turn on device, wherein the on-screen display turn on device causes the frames encoded with the on-screen display to be supplied to a digital television in response to the on-screen display I frame marker, and wherein the on-screen display turn on device causes the original video frames to be supplied to the digital television in response to the video I frame marker.

10. The MPEG on-screen display coder of claim 9 wherein the MPEG encoder signals the on-screen display I frame marker when the MPEG encoder generates an encoded I frame, and wherein the MPEG encoder signals the video I frame marker when an original I frame is received.

11. The MPEG on-screen display coder of claim 1 wherein the on-screen display is overlaid on video.

12. The MPEG on-screen display coder of claim 11 wherein the MPEG encoder is arranged to pass unchanged I frames.

13. The MPEG on-screen display coder of claim 12 wherein the MPEG encoder is arranged to encode a first P frame by predicting the first P frame from a preceding I frame with residuals in the predicted first P frame containing the on-screen display and with motion vectors set equal to zero, and wherein the MPEG encoder is arranged to encode subsequent P frames based upon the predicted first P frame with residuals and motion vectors set equal to zero.

14. The MPEG on-screen display coder of claim 13 wherein the MPEG encoder is arranged to supply first and second I frame markers to the on-screen display turn on device, wherein the on-screen display turn on device causes the frames encoded with the on-screen display to be supplied to a digital television in response to the first I frame marker, and wherein the on-screen display turn on device causes original video frames to be supplied to the digital television in response to the second I frame marker.

15. The MPEG on-screen display coder of claim 14 wherein the MPEG encoder signals the first and second I frame markers when corresponding original I frames are received.

16. The MPEG on-screen display coder of claim 11 wherein the MPEG encoder is arranged to encode I frames with the on-screen display.

17. The MPEG on-screen display coder of claim 16 wherein the MPEG encoder is arranged to encode subsequent P frames by prediction based upon the encoded I frames with residuals and motion vectors set equal to zero.

18. The MPEG on-screen display coder of claim 17 wherein the MPEG encoder is arranged to supply first and second I frame markers to the on-screen display turn on device, wherein the on-screen display turn on device causes the frames encoded with the on-screen display to be supplied to a digital television in response to the first I frame marker, and wherein the on-screen display turn on device causes original frames to be supplied to the digital television in response to the second I frame marker.

19. The MPEG on-screen display coder of claim 18 wherein the MPEG encoder signals the first and second I frame markers when corresponding original I frames are received.

20. The MPEG on-screen display coder of claim 1 wherein the MPEG encoder is arranged to generate an I frame having a solid color background and an on-screen display, and wherein the MPEG encoder generates a P frame predicted from the I frame with residuals and motion vectors set equal to zero.

21. The MPEG on-screen display coder of claim 1 wherein the MPEG encoder is arranged to encode frames with the on-screen display by prediction with non-zero motion vectors in order to encode animated graphics.

22. The MPEG on-screen display coder of claim 1 wherein the MPEG encoder is arranged to pass a first I frame without modification, to predict subsequent P frames based upon the first I frame, to overlay the on-screen display on a second I frame, and to predict subsequent P frames based upon the second I frame.

23. The MPEG on-screen display coder of claim 1 wherein the MPEG encoder is arranged to encode frames by mixing original video in a window of reduced size with the on-screen display.

24. The MPEG on-screen display coder of claim 1 wherein the MPEG encoder is arranged to pass unchanged I frames.

25. The MPEG on-screen display coder of claim 24 wherein the MPEG encoder is arranged to encode a first P frame by predicting the first P frame from a preceding I frame with residuals in the predicted first P frame containing the on-screen display and with motion vectors set equal to zero, and wherein the MPEG encoder is arranged to encode subsequent P frames based upon the predicted first P frame with residuals and motion vectors set equal to zero.

26. The MPEG on-screen display coder of claim 25 wherein the MPEG encoder is arranged to supply first and second I frame markers to the on-screen display turn on device, wherein the on-screen display turn on device causes the frames encoded with the on-screen display to be supplied to a digital television in response to the first I frame marker, and wherein the on-screen display turn on device causes original frames to be supplied to the digital television in response to the second I frame marker.

27. The MPEG on-screen display coder of claim 26 wherein the MPEG encoder signals the first and second I frame markers when corresponding original I frames are received.

28. The MPEG on-screen display coder of claim 1 wherein the MPEG encoder is arranged to encode I frames with the on-screen display.

29. The MPEG on-screen display coder of claim 28 wherein the MPEG encoder is arranged to encode subsequent P frames by prediction based upon the encoded I frames with residuals and motion vectors set equal to zero.

30. The MPEG on-screen display coder of claim 29 wherein the MPEG encoder is arranged to supply first and second I frame markers to the on-screen display turn on device, wherein the on-screen display turn on device causes the frames encoded with the on-screen display to be supplied to a digital television in response to the first I frame marker, and wherein the on-screen display turn on device causes original frames to be supplied to the digital television in response to the second I frame marker.

31. The MPEG on-screen display coder of claim 30 wherein the MPEG encoder signals the first and second I frame markers when corresponding original I frames are received.

32. An MPEG on-screen display coder comprising:

an MPEG encoder arranged to encode frames of a selected program with an on-screen display; and,

a multiplexer arranged to replace original frames with the encoded frames for supply to a digital television receiver.

33. The MPEG on-screen display coder of claim 32 wherein the encoded frames have a time base which is independent of the original frames.

34. The MPEG on-screen display coder of claim 33 wherein the on-screen display is overlaid on a solid color background.

35. The MPEG on-screen display coder of claim 33 wherein the MPEG encoder is arranged to calculate a video hold off time dependent upon a number of frames in a decoder buffer of the digital television receiver and to use the video hold off time so as to prevent overflow of the decoder buffer.

36. The MPEG on-screen display coder of claim 35 wherein the MPEG encoder controls the multiplexer with the video hold off time so as to permit the encoded frames to be supplied to the digital television receiver when the video hold off time expires.

37. The MPEG on-screen display coder of claim 32 wherein the encoded frames have a time base which is slaved to the original frames.

38. The MPEG on-screen display coder of claim 37 wherein the on-screen display is overlaid on a solid color background.

39. The MPEG on-screen display coder of claim 37 wherein the MPEG encoder is arranged to supply I frame markers, and wherein the multiplexer is controlled in response to the I frame markers so as to begin supplying encoded frames to the digital television receiver with one I frame and to resume supplying the original frames to the digital television receiver with another I frame.

40. The MPEG on-screen display coder of claim 37 wherein the MPEG encoder is arranged to supply a video I frame marker and an on-screen display I frame marker, wherein the multiplexer is controlled in response to the on-screen display I frame marker so as to begin supplying encoded frames to the digital television receiver with one I frame, and wherein the multiplexer is controlled in response to the video I frame marker so as to resume supplying the original frames to the digital television receiver with another I frame.

41. The MPEG on-screen display coder of claim 40 wherein the MPEG encoder supplies the on-screen display I frame marker when the MPEG encoder generates an encoded I frame, and wherein the MPEG encoder signals the video I frame marker when an original I frame is received.

42. The MPEG on-screen display coder of claim 32 wherein the on-screen display is overlaid on video.

43. The MPEG on-screen display coder of claim 42 wherein the MPEG encoder is arranged to pass unchanged I frames.

44. The MPEG on-screen display coder of claim 43 wherein the MPEG encoder is arranged to encode a first P frame by predicting the first P frame from a preceding I frame with residuals in the predicted first P frame containing the on-screen display and with motion vectors set equal to zero, and wherein the MPEG encoder is arranged to encode subsequent P frames based upon the predicted first P frame with residuals and motion vectors set equal to zero.

45. The MPEG on-screen display coder of claim 44 wherein the MPEG encoder is arranged to supply first and second I frame markers, wherein the multiplexer is controlled in response to the first I frame marker so as to begin supplying encoded frames to the digital television receiver with one I frame, and wherein the multiplexer is controlled in response to the second I frame marker so as to resume supplying the original frames to the digital television receiver with another I frame.

46. The MPEG on-screen display coder of claim 42 wherein the MPEG encoder is arranged to encode I frames with the on-screen display.

47. The MPEG on-screen display coder of claim 46 wherein the MPEG encoder is arranged to encode subsequent P frames by prediction based upon the encoded I frames with residuals and motion vectors set equal to zero.

48. The MPEG on-screen display coder of claim 47 wherein the MPEG encoder is arranged to supply first and second I frame markers, wherein the multiplexer is controlled in response to the first I frame marker so as to begin supplying encoded frames to the digital television receiver with one I frame, and wherein the multiplexer is controlled in response to the second I frame marker so as to resume supplying the original frames to the digital television receiver with another I frame.

49. The MPEG on-screen display coder of claim 32 wherein the MPEG encoder is arranged to generate an I frame having a solid color background and an on-screen display, and wherein the MPEG encoder generates a P frame predicted from the I frame with residuals set equal to zero.

50. The MPEG on-screen display coder of claim 32 wherein the MPEG encoder is arranged to encode frames with the on-screen display by prediction with non-zero motion vectors in order to encode animated graphics.

51. The MPEG on-screen display coder of claim 32 wherein the MPEG encoder is arranged to pass a first I frame without modification, to predict subsequent P frames based upon the first I frame, to overlay the on-screen display on a second I frame, and to predict subsequent P frames based upon the second I frame.

52. The MPEG on-screen display coder of claim 32 wherein the MPEG encoder is arranged to encode frames by mixing original video in a window of reduced size with the on-screen display.

53. The MPEG on-screen display coder of claim 32 wherein the MPEG encoder is arranged to pass unchanged I frames.

54. The MPEG on-screen display coder of claim 53 wherein the MPEG encoder is arranged to encode a first P frame by predicting the first P frame from a preceding I frame with residuals in the predicted first P frame containing the on-screen display and with motion vectors set equal to zero, and wherein the MPEG encoder is arranged to encode subsequent P frames based upon the predicted first P frame with residuals and motion vectors set equal to zero.

55. The MPEG on-screen display coder of claim 54 wherein the MPEG encoder is arranged to supply first and second I frame markers, wherein the multiplexer is controlled in response to the first I frame marker so as to begin supplying encoded frames to the digital television receiver with one I frame, and wherein the multiplexer is controlled in response to the second I frame marker so as to resume supplying the original frames to the digital television receiver with another I frame.

56. The MPEG on-screen display coder of claim 32 wherein the MPEG encoder is arranged to encode I frames with the on-screen display.

57. The MPEG on-screen display coder of claim 56 wherein the MPEG encoder is arranged to encode subsequent P frames by prediction based upon the encoded I frames with residuals and motion vectors set equal to zero.

58. The MPEG on-screen display coder of claim 57 wherein the MPEG encoder is arranged to supply first and second I frame markers, wherein the multiplexer is controlled in response to the first I frame marker so as to begin supplying encoded frames to the digital television receiver with one I frame, and wherein the multiplexer is controlled in response to the second I frame marker so as to resume supplying the original frames to the digital television receiver with another I frame.

59. The MPEG on-screen display coder of claim 32 wherein the multiplexer is arranged to add make-up packets to each encoded frame as necessary to ensure that each encoded frame has as many transport packets as the original frames.

60. The MPEG on-screen display coder of claim 59 wherein the make-up packets are null packets.

61. The MPEG on-screen display coder of claim 59 wherein the make-up packets are Program Map Table packets.

62. An MPEG on-screen display coder comprising:

a buffer arranged to receive and buffer an MPEG transport data stream containing frames of a selected program and frames of a non-selected program;

an MPEG encoder arranged to encode frames of the selected program with an on-screen display; and,

a multiplexer arranged to selectively pass to a digital television receiver the frames of the non-selected program, the encoded frames of the selected program, and original frames of the selected program.

63. The MPEG on-screen display coder of claim 62 wherein the encoded frames have a time base which is independent of the original frames of the selected program.

64. The MPEG on-screen display coder of claim 62 wherein the encoded frames have a time base which is slaved to the original frames of the selected program.

65. The MPEG on-screen display coder of claim 62 wherein the MPEG encoder is arranged to calculate a video hold off time dependent upon a number of frames in a decoder buffer of the digital television receiver and to use the video hold off time so as to prevent overflow of the decoder buffer.

66. The MPEG on-screen display coder of claim 62 wherein the MPEG encoder is arranged to supply I frame markers, and wherein the multiplexer is controlled in response to the I frame markers so as to begin supplying encoded frames to the digital television receiver with one I frame and to resume supplying the original frames of the selected program to the digital television receiver with another I frame.

67. The MPEG on-screen display coder of claim 62 wherein the MPEG encoder is arranged to supply a video I frame marker and an on-screen display I frame marker, wherein the multiplexer is controlled in response to the on-screen display I frame marker so as to begin supplying encoded frames to the digital television receiver with one I frame, and wherein the multiplexer is controlled in response to the video I frame marker so as to resume supplying the

original frames of the selected program to the digital television receiver with another I frame.

68. The MPEG on-screen display coder of claim 67 wherein the MPEG encoder supplies the on-screen display I frame marker when the MPEG encoder generates an encoded I frame, and wherein the MPEG encoder signals the video I frame marker when an original I frame of the selected program is received.

69. The MPEG on-screen display coder of claim 62 wherein the on-screen display is overlaid on a solid color background.

70. The MPEG on-screen display coder of claim 62 wherein the on-screen display is overlaid on video.

71. The MPEG on-screen display coder of claim 62 wherein the MPEG encoder is arranged to pass unchanged I frames.

72. The MPEG on-screen display coder of claim 71 wherein the MPEG encoder is arranged to encode a first P frame by predicting the first P frame from a preceding I frame with residuals in the predicted first P frame containing the on-screen display and with motion vectors set equal to zero, and wherein the MPEG encoder is arranged to encode subsequent P frames based upon the predicted first P frame with residuals and motion vectors set equal to zero.

73. The MPEG on-screen display coder of claim 72 wherein the MPEG encoder is arranged to supply first and second I frame markers, wherein the multiplexer is controlled in response to the first I frame marker so as to begin supplying the encoded frames to the digital television receiver with one I frame, and wherein the multiplexer is controlled in response to the second I frame marker so as to resume supplying the original frames of the selected program to the digital television receiver with another I frame.

74. The MPEG on-screen display coder of claim 62 wherein the MPEG encoder is arranged to encode I frames with the on-screen display.

75. The MPEG on-screen display coder of claim 74 wherein the MPEG encoder is arranged to encode subsequent P frames by prediction based upon the encoded I frames with residuals and motion vectors set equal to zero.

76. The MPEG on-screen display coder of claim 75 wherein the MPEG encoder is arranged to supply first and second I frame markers, wherein the multiplexer is controlled in response to the first I frame marker so as to begin supplying the encoded frames to the digital television receiver with one I frame, and wherein the multiplexer is controlled in response to the second I frame marker so as to resume supplying the original frames of the selected program to the digital television receiver with another I frame.

77. The MPEG on-screen display coder of claim 62 wherein the MPEG encoder is arranged to generate an I frame having a solid color background and an on-screen display, and wherein the MPEG encoder generates a P frame predicted from the I frame with zero residual.

78. The MPEG on-screen display coder of claim 62 wherein the MPEG encoder is arranged to encode frames with the on-screen display by prediction with non-zero motion vectors in order to encode animated graphics.

79. The MPEG on-screen display coder of claim 62 wherein the MPEG encoder is arranged to pass a first I frame without modification, to predict subsequent P frames based upon the first I frame, to overlay the on-screen display on a second I frame, and to predict subsequent P frames based upon the second I frame.

80. The MPEG on-screen display coder of claim 62 wherein the MPEG encoder is arranged to encode frames by mixing original video of the selected program in a window of reduced size with the on-screen display.

81. The MPEG on-screen display coder of claim 62 wherein the multiplexer is arranged to add make-up packets to each encoded frame as necessary to ensure that each encoded frame has as many transport packets as an original frame of the selected program.

82. The MPEG on-screen display coder of claim 81 wherein the make-up packets are null packets.

83. The MPEG on-screen display coder of claim 81 wherein the make-up packets are Program Map Table packets.